Notice of Allowability	Application No.	Applicant(s)	
	10/797,245	DATE ET AL.	
	Examiner	Art Unit	
	Richard V. Muralidar	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/11/2004*.

2. ☒ The allowed claim(s) is/are *1-31*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3-11-2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

REASONS FOR ALLOWANCE

The following is the examiner's statement of reasons for allowance. The prior art does not disclose or suggest the following Claim 1 limitations: "a current driving device provided on a semiconductor chip, comprising: a first-conductive-type first MISFET to which from a reference current source for making a reference current flow, the reference current is transmitted; a first-conductive-type current distribution MISFET which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow," nor "a reference current output terminal which is provided on a region of the semiconductor chip located at a distance of 200 micrometers or less from the current transmission MISFET and outputs a current transmitted from the current transmission MISFET" in combination with the remaining claim elements as set forth in Claim 1.

The prior art does not disclose or suggest the following Claim 12 limitations: "a second-conductive-type first current input MISFET having a drain connected to the first current distribution MISFET; and a plurality of current supply sections each including second-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data, and an output terminal which is connected to the switches and outputs a current in accordance with the display data to a display panel, the current driving device being provided on a semiconductor chip, wherein a plurality of units of the first current distribution MISFET and the first current input

MISFET are provided for the semiconductor chip, and wherein a bias line connected to a gate electrode of the first MISFET and gate electrodes of the first current distribution MISFETs and shared by the gate electrodes is further provided" in combination with the remaining claim elements as set forth in Claim 12.

The prior art does not disclose or suggest the following Claim 24 limitations: "a first-conductive-type first current input MISFET in which a first reference current flows in a driving state; a first-conductive-type second current input MISFET in which a second reference current flows in a driving state; and a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data, a first-conductive-type cascode MISFET which is provided between the current source MISFETs and one of the switches and constitutes a current mirror circuit together with the second current input MISFET" in combination with the remaining claim elements as set forth in Claim 24.

The prior art does not disclose or suggest the following Claim 26 limitations: "a first-conductive-type second current input MISFET in which a second reference current flows in a driving state; and a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data, a first-conductive-type cascode MISFET which is

provided between the current source MISFETs and one of the switches and constitutes a current mirror circuit together with the second current input MISFET, and an output terminal which is connected to the switches and outputs a current in accordance with the display data, the current driving device being provided on a semiconductor chip" in combination with the remaining claim elements as set forth in Claim 26.

The prior art does not disclose or suggest the following Claim 28 limitations: "each of the plurality of the semiconductor chips includes a reference current input terminal for receiving a reference current in an end portion and a reference current output terminal for outputting a reference current for a semiconductor chip in a subsequent stage in another end portion, and wherein the reference current input terminal and the reference current output terminal located in adjacent ones of the plurality of the semiconductor chips, respectively, are provided so as to face each other" in combination with the remaining claim elements as set forth in Claim 28.

The prior art does not disclose or suggest the following Claim 29 limitations: "wherein the current driving device includes a first-conductive-type first MISFET in which a reference current flows in a driving state, a plurality of first-conductive-type current distribution MISFETs which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow, a plurality of second-conductive-type current input MISFETs each having a drain connected to each of the plurality of the current distribution MISFETs, and a plurality of current supply sections each including second-conductive-type current source MISFETs constituting a current mirror circuit together with the current input MISFET and an output terminal for outputting to

the pixel circuit a driving current in accordance with the display data" in combination with the remaining claim elements as set forth in Claim 29.

The prior art does not disclose or suggest the following Claim 30 limitations: "a plurality of semiconductor chips each including a current driving device for supplying a driving current to the pixel circuit, wherein the current driving device includes a first-conductive-type first current input MISFET in which a first reference current flows in a driving state, a first-conductive-type second current input MISFET in which a second reference current flows in a driving state, and a plurality of current supply sections each including first-conductive-type current source MISFETs constituting a current mirror circuit together with the first current input MISFET, switches which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data" in combination with the remaining claim elements as set forth in Claim 30.

The prior art made of record in the attached PTO-892 is considered to be pertinent to the submitted application.

Koyama [US 6777885] discloses a drive circuit for a display device that comprises numerous switches that utilize an organic layer, in conjunction with a reference current source and current control means. Koyama does not disclose or suggest the use of MISFETs to perform the current control/driving circuit, nor a reference current output terminal provided on a region of a semiconductor chip located at a distance of 200 micrometers or less from a current transmission MISFET.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "comments on statement of reasons for allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard V. Muralidar whose telephone number is 571-272-8933. The examiner can normally be reached on Monday to Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on Monday to Friday 8-5. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RVM
4/28/2006

DAVID M. GRAY
PRIMARY EXAMINER